Professional Biography of
Stephen Flannagan

Stephen T. Flannagan received the BSEE degree with honors at the University of Cincinnati in 1977, where he designed and fabricated MOS circuits. His student employment included the design of digital communication circuits. He received the MSEE from Oregon State University, concurrently while employed at Intel. His thesis topic, "Synchronization Reliability in CMOS Technology," was later published in the IEEE Journal of Solid-State Circuits.

From 1977 to 1979 he was with Intel in Santa Clara, California, as Product Engineer for EPROM devices. From 1979 to 1983 he was with Intel in Aloha, Oregon, where he designed the critical synchronization and control circuits for the world's first commercial pseudostatic RAM products at 64K density.

In 1983 he joined Motorola in Austin, Texas, where he was responsible for design and development of some of the world's fastest CMOS static RAM products. He originated several new design techniques and a new chip architecture, which have since become widely used throughout the world in state-of-the-art memory design. These techniques include memory designs that are immune to timing variations in addresses and control signals, input buffers with hysteresis and dc margin for tolerance of address-float and other asynchronous bus conditions, and analog data amplification techniques.

He and his team introduced high-speed CMOS static RAMs at the 64K density in 1986, the 256K density in 1989, and a family of ultra-high-speed BiCMOS SRAMs at 1-Meg density in 1991. Each generation of SRAM was recognized as the fastest commercially available SRAM of its type in the world in volume production. The fast SRAMs were designed in multiple formats, with both TTL and ECL interfaces, word-width from x1 to x36, and with input/output levels tuned to match their environments and with voltage levels that differ from the chip supply.

In 1993 the Motorola Fast Static RAM division was recognized as the number one producer of fast (sub 70-ns) static RAMs in the world, and this dominance was maintained for the years 1993 through 1996, as independently verified by industry monitors, reaching a peak of more than $500 million in sales per year.

From 1992-1993, Steve also directed the team that developed a unique multi-stage pipelined SRAM at 4-Meg density, for use in a specialized application for ultra-high-speed computation. These special SRAMs used phase-locking techniques to regularize the edges of clocks from one part of the chip to another, and used specialized output synchronizing techniques. These innovations permitted memory operating frequencies significantly faster than originally targeted by the process technology.

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From 1994-1999, Steve directed teams which developed and introduced into production several families of SRAM at the 4-Meg and 8-Meg densities, with coherent-write-cycle bus interfaces for engineering workstations and other applications. His teams designed various specialized circuits including a new generation of highly efficient and noise-free on-chip power regulation circuits.

From 2000-2001, Steve designed and directed the development of specialized SRAM circuits for embedding in baseband communication circuits. This activity included complex circuits such as embedded testability and redundancy, electrically programmable fuses, multiple on-chip supply regulation, and ultra-low-power techniques.

Steve was awarded the title of "Fellow" at Motorola in 1988, the highest technical honor bestowed on company employees. He was recognized in the Corporation's 1989 Annual Report to Stockholders. He was given the "Distinguished Innovator" award and membership in the Science Advisory Board Associates. He and his co-authors were granted the 1986-1987 Best Paper Award by the IEEE Journal of Solid-State Circuits. He organized and chaired the evening panel session "Large-Scale Integration versus Multi-chip Modules" at the 1995 International Solid-State Circuits Conference, which included six extremely distinguished panelists from industry and academia, including chip designers and system designers. Steve holds about 40 United States Patents and numerous patents in other countries. He presented an invited paper at the 1988 IEDM conference entitled "Future Technology Trends for Static RAMs," and has authored numerous papers in refereed Journals. He has given invited talks at universities on circuit design, and his published work has been used as material in university courses on design techniques.

Steve has hired, trained and mentored several dozen of the finest technical professionals in the industry. Most persons who have worked for him have advanced to high positions at various companies, and have been recognized for some very remarkable achievements. Several are high-level managers, two are directors of design, and another became a vice-president.

Steve is known for his helpfulness to persons at all levels, including his subordinates, co-workers, and superiors. He is extremely supportive of all persons that he works with, and works tirelessly to help his team members and superiors to achieve world-class success. He initiated and guided several programs for advancing professionalism and career development for engineers, layout designers and CAD specialists in integrated circuit design.

In 2002, Steve founded "Flannagan I.C. Technical Services and Consulting, Inc.," dedicated to helping his clients achieve spectacular success with Integrated Circuits. He has supported major industry projects in such areas as on-chip regulation, charge pump design, memory redundancy and synchronization.